In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown in accordance with the mandatory amendment format.

1. (Currently Amended) An apparatus, comprising:

a test controller, coupled between a bus and first and second cores in a multi-core computer, to operate a data flow stress test in the multi-core computer, the test controller having:

a first multiplexer coupled between the first core and the bus;

a second multiplexer coupled between the second core and the bus;

a register to store test information; and

a control circuit coupled between the register and the first and second multiplexers.

2. (Currently Amended) The apparatus of claim 1, wherein the test controller includes:

a test request library; and

a detection library.

~~a first multiplexer coupled between the first core and the bus;~~

~~a second multiplexer coupled between the second core and the bus;~~

~~a register to store test information; and~~

~~a control circuit coupled between the register and the first and second multiplexers.~~

3. (Currently Amended) The apparatus of claim 1 ~~2~~, wherein:

the control circuit is to select an input of the first multiplexer between a first data request from the first core and a test data request from the control circuit.

4. (Currently Amended) The apparatus of claim 1 ~~2~~, wherein:

the control circuit is to select an input of the second multiplexer between a first data request from the second core and a test data request from the control circuit.

5. (Original) The apparatus of claim 1, wherein:

the test controller is to be electrically deactivated after the stress test.

6. (Original) The apparatus of claim 1, wherein:

the test controller, first core, and second core are all disposed on a same integrated circuit.

7. (Currently Amended) A system comprising:

a memory;

a multi-core computer coupled to the memory; and

a test controller, coupled between a bus and first and second cores in the multi-core computer, to operate a data flow stress test in the multi-core computer, the test controller having:

first switching logic coupled between the first core and the bus;

second switching logic coupled between the second core and the bus;

a register to store test information; and

a control circuit coupled between the register and the first and second switching logic.

8. (Currently Amended) The system of claim 7, wherein the test controller includes a test request library.~~:~~

~~switching logic to switch the bus between data requests from at least one of the first and second cores and test data requests from the test controller.~~

9. (Currently Amended) The system of claim 7, wherein the test controller includes a detection library.~~:~~

~~the test controller includes a register to store test information.~~

10. (Original) The system of claim 7, wherein:

the test controller is to be electrically deactivated after the stress test.

11. (Original) The system of claim 7, wherein:

the test controller, first core, and second core are all disposed on a same integrated circuit.

12. (Currently Amended) A method comprising:

~~stress testing a multi-core computer by blocking a first data request from a first core to a bus and sending a test data request from a test controller to the bus.~~

receiving test setup information at an integrated circuit via an integrated test port;

initiating a test upon detecting that a data request passing through a bus controller matches a data request at a detection library;

issuing a test data request; and

writing test result data to a test register.

13. (Currently Amended) The method of claim 12, wherein receiving test setup information further comprises:

writing a detection index to the test register;

writing a response index to the test register; and

writing an on code into the test register.

~~the stress testing further includes sending a second data request from a second core to the bus.~~

14. (Currently Amended) The method of claim 12, further comprising ~~wherein~~:

blocking data requests issued at a first processor and a second processor after initiating the test.

~~the blocking and the sending are controlled by a test controller.~~

15. (Currently Amended) The method of claim 12, further comprising reading the test result data from the test register ~~wherein~~:

~~the test data request is selected by a test register.~~

16. (Currently Amended) The method of claim 12, further comprising writing an off code into the test register to terminate the test~~wherein~~:

~~the stress testing further includes blocking a second data request from a second core to the bus.~~

17. (Currently Amended) A machine-readable medium that provides instructions, which when executed by a set of one or more processors, cause said set of processors to perform operations comprising:

~~stress testing a multi-core computer by blocking a first data request from a first core to a bus and sending a test data request from a test controller to the bus.~~

receiving test setup information at an integrated circuit via an integrated test port;

initiating a test upon detecting that a data request passing through a bus controller matches a data request at a detection library;

issuing a test data request; and

writing test result data to a test register.

18. (Currently Amended) The medium of claim 17, wherein receiving test setup information further comprises:

writing a detection index to the test register;

writing a response index to the test register; and

writing an on code into the test register.

~~the stress testing further includes sending a second data request from a second core to the bus.~~

19. (Currently Amended) The medium of claim 17, further comprising ~~wherein~~:

blocking data requests issued at a first processor and a second processor after initiating the test.

~~the blocking and the sending are controlled by a test controller.~~

20. (Currently Amended) The medium of claim 17, further comprising reading the test result data from the test register ~~wherein~~:

~~the test data request is selected by a test register.~~

21. (Currently Amended) The medium of claim 17, further comprising writing an off code into the test register to terminate the test~~wherein~~:

~~the stress testing further includes blocking a second data request from a second core to the bus.~~

22. (Original) A machine-readable medium that provides instructions, which when executed by a set of one or more processors, cause said set of processors to perform operations comprising:

obtaining test data for stress testing a multi-core computer system;

writing the test data to a test register in the multi-core computer system through a test port; and

reading a test result from the test register through the test port.

23. (Original) The medium of claim 22, wherein:

said writing includes writing an 'on' bit to the test register.

24. (Original) The medium of claim 22, wherein:

said writing includes specifying data requests to be monitored as triggers to start a test.

25. (Original) The medium of claim 22, wherein:

said writing includes specifying test data requests to be issued.